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METHOD OF REDUCING INSTANTANEOUS CURRENT DRAW AND AN INTEGRATED CIRCUIT MADE THEREBY

Abstract

A method (200, 300, 400, 500) utilizing available timing slack in the various timing paths (108) of a synchronous integrated circuit (104) to reduce the overall instantaneous current draw across the circuit. In the method, each timing path is analyzed to determine its late mode margin or its late mode margin and early mode margin. A delay is added to each timing path having a late mode margin greater than zero. In one embodiment, the delay is equal to the corresponding late mode margin. In another embodiment, the delay is equal to the difference between the corresponding late and early mode margins. Each delay effectively shifts the peak current draw for the corresponding timing path within each clock cycle so that the peaks do not occur simultaneously across all timing paths. In other embodiments, the peak overall instantaneous current draw can be further reduced by reducing the delay in some of the delayed timing paths.